ATTACHMENT
OFFICE ACTION RESPONSE MAILED 8/22/2005

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Please stamp and return this postcard to acknowledge receipt of a paper responsive to an Office Action against, "Ultra-Shallow Metal Oxide Surface Channel MOS Transistor", invented by Li et al., Serial No. 10/761,704, along with a check in the amount of $200, being mailed August 22, 2005.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:		) ATTORNEY FILE NO.:
Inventors:	Li et al.	) SLA0845
Serial No.:	10/761,704	) Examiner: Erdem, Fazli
Filed:	January 21, 2004	) Customer No.: 55,286
Title:	ULTRA-SHALLOW METAL OXIDE SURFACE CHANNEL MOS TRANSISTOR	) Group Art: 2826) Confirmation No.: 3680

MAIL STOP AMENDMENTS
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CERTIFICATION UNDER 37 CFR § 1.8

I hereby certify that the documents referred to as enclosed herein are being deposited with the United States Postal Service as first class mail on this date 8/22/2005, in an envelope addressed to: Mail Stop Amendments, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date 8/19/2005 Signature

AMENDMENT AND REQUEST FOR RECONSIDERATION UNDER 37 CFR 1.111

In response to an Office Action filed June 30, 2005, please amend and reconsider the above-referenced application as follows.

Amendments to the claims begin at page 2 of this paper.

Remarks begin at page 9 of this paper.

An Associate Power of Attorney is enclosed as Attachment A.

A fee transmittal sheet is enclosed as Attachment B.

IN THE CLAIMS:

1. (Previously Presented) A method for fabricating an ultra-shallow surface channel MOS transistor, the method comprising:

forming CMOS source and drain regions, and an intervening well region with a surface;

depositing a metal oxide surface channel on the surface overlying the well region, selected from the group of materials including indium oxide (In_2O_3), ZnO, RuO, ITO, and $La_{x-1}Sr_xCoO_3$;

forming a high-k dielectric, having a thickness in the range of 1 to 5nm, overlying the surface channel; and,

forming a gate electrode overlying the high-k dielectric.

2-3. Canceled

4. (Previously Presented) A method for fabricating an ultra-shallow surface channel MOS transistor, the method comprising:

forming CMOS source and drain regions, and an intervening well region with a surface;

depositing a surface channel on the surface overlying the well region;

forming a high-k dielectric overlying the surface channel;

depositing a placeholder material overlying the surface channel;

conformally depositing oxide;

etching the placeholder material to form a gate region overlying the surface channel; and,

forming a gate electrode overlying the high-k dielectric in the gate region.

5. (Original) The method of claim 4 further comprising:

following the deposition of the placeholder material, lightly doped drain (LDD) processing the source and drain regions;

wherein forming a high-k dielectric insulator overlying the surface channel includes depositing the high-k dielectric prior to the deposition of the placeholder material;

the method further comprising:

forming sidewall insulators adjacent the surface channel, high-k dielectric insulator, and gate region; and,

heavy ion implanting and activating the source and drain regions.

6. (Original) The method of claim 4 further comprising:

prior to the deposition of the surface channel, lightly doped drain (LDD) processing the source and drain regions;

heavy ion implanting and activating the source and drain regions; and,

wherein forming a high-k dielectric insulator overlying the surface channel includes depositing the high-k dielectric following the etching of the placeholder material to form the gate region.

7. (Previously Presented) A method for fabricating an ultra-shallow surface channel MOS transistor, the method comprising:

forming CMOS source and drain regions, and an intervening well region with a surface;

depositing a metal oxide surface channel on the surface overlying the well region having a thickness in the range in the range of 10 to 20 nanometers (nm);

forming a high-k dielectric overlying the surface channel; and,

forming a gate electrode overlying the high-k dielectric.

8. (Previously Presented) A method for fabricating an ultra-shallow surface channel MOS transistor, the method comprising:

forming CMOS source and drain regions, and an intervening well region with a surface;

depositing a metal oxide surface channel on the surface overlying the well region having a resistivity in the range between 0.1 and 1000 ohm-cm;

forming a high-k dielectric overlying the surface channel; and,

forming a gate electrode overlying the high-k dielectric.

9. (Original) The method of claim 1 wherein forming a high-k dielectric insulator overlying the surface channel includes depositing a high-k dielectric material selected from the group including HfO_2, HfAlOx, ZrO_2, and Al_3O_4.

10. Canceled

11. (Original) The method of claim 4 wherein depositing a placeholder material overlying the surface channel includes forming placeholder material to a first thickness with a placeholder material surface; and,

wherein conformally depositing oxide includes depositing oxide to a second thickness in the range of 1.2 to 1.5 times the first thickness; and,

the method further comprising:

chemical mechanical polishing (CMP) the oxide to the level of the placeholder material surface.

12. (Original) The method of claim 5 wherein forming sidewall insulators adjacent the surface channel, high-k dielectric insulator, and gate region includes forming sidewalls from a material selected from the group including Si_3N_4 and Al_2O_3.

13. (Previously Presented) An ultra-shallow surface channel MOS transistor, the transistor comprising:

a source region;

a drain region;

a well region intervening between the source and drain with a surface;

a metal oxide surface channel overlying the well region, selected from a group of materials including indium oxide (In_2O_3), ZnO, RuO, ITO, and $La_{x-1}Sr_xCoO_3$;

a high-k dielectric insulator, having a thickness in the range of 1 to 5 nm, overlying the surface channel; and,

a gate electrode overlying the high-k dielectric layer.

14-15. Canceled

16. (Previously Presented) An ultra-shallow surface channel MOS transistor, the transistor comprising:

a source region;

a drain region;

a well region intervening between the source and drain with a surface;

a surface channel overlying the well region;

a high-k dielectric insulator overlying the surface channel;

a placeholder overlying the surface channel, forming a temporary gate region; and,

a gate electrode overlying the high-k dielectric layer, formed in the gate region.

17. (Original) The transistor of claim 16 wherein the placeholder is temporarily formed directly overlying the high-k dielectric insulator;

the transistor further comprising:

sidewall insulators adjacent the surface channel, high-k dielectric insulator, and the gate region.

18. (Original) The transistor of claim 16 wherein the placeholder is temporarily formed directly overlying the surface channel.

19. (Previously Presented) An ultra-shallow surface channel MOS transistor, the transistor comprising:

a source region;

a drain region;

a well region intervening between the source and drain with a surface;

a metal oxide surface channel overlying the well region having a thickness in the range in the range of 10 to 20 nanometers (nm);

a high-k dielectric insulator overlying the surface channel; and

a gate electrode overlying the high-k dielectric layer.

20. (Previously Presented) An ultra-shallow surface channel MOS transistor, the transistor comprising:

a source region;

a drain region;

a well region intervening between the source and drain with a surface;

a metal oxide surface channel overlying the well region having a resistivity in the range between 0.1 and 1000 ohm-cm;

a high-k dielectric insulator overlying the surface channel; and

a gate electrode overlying the high-k dielectric layer.

21. (Original) The transistor of claim 13 wherein the high-k dielectric insulator is a material selected from the group including HfO_2, HfAlOx, ZrO_2, and Al_3O_4.

22. Canceled

23. (Original) The transistor of claim 17 wherein the sidewall insulators are a material selected from the group including Si_3N_4 and Al_2O_3.

24. (New) A method for fabricating an ultra-shallow surface channel MOS transistor, the method comprising:

forming CMOS source and drain regions, and an intervening well region with a surface;

depositing a metal oxide surface channel on the surface overlying the well region;

forming a high-k dielectric; and,

forming a gate electrode overlying the high-k dielectric.

REMARKS

This paper is responsive to an Office Action dated June 30, 2005. Prior to this response, claims 1, 4-13, 16-21, and 23 were pending. After adding claim 24, claims 1, 4-13, 16-21, and 23-24 remain pending.

Section 1 of the Office Action states that claims 4-8, 11-12, and 16-20 have been allowed.

Section 2 of the Office Action states that claim 23 would be found allowable if rewritten in independent form including all the subject matter of the base and intervening claims. Claim 23 depends from claims 16 and 17, both of which have been allowed. Therefore, the Applicant assumes that claim 23 is also allowable as presented.

Section 3 of the Office Action states that claims 1, 9, 13, and 21 have been rejected as unpatentable under 35 U.S.C. 103(a) with respect to Kim et al. (6,621,114), in view of Currie et al. (2003/0234439) and Sohn et al. (6,753,230), and further in view of Hoffman (2004/0155846) and Rotondaro et al. ("Rotondaro"; US 6,656,852). The Office Action acknowledges that Kim fails to describe a surface channel, a high-k dielectric overlying the surface channel, or the recited high-k dielectric thickness. The Office Action states that Currie and Sohn describe surface channels, that Hoffman describes a metal oxide material, and that Rotondaro describes a high-k dielectric thickness of greater than 1 nm. The Office Action states that, "it would have been obvious to one having ordinary skill at the time of the invention to include the required surface channel, the required ultra-shallow channel structures, the required metal oxides, and the required high-k dielectric thickness in Kim et al. as taught by Currie et al., Sohn et al., Hoffman et al., and Rotondaro

et al. in order to have a semiconductor device with increased performance. This rejection is traversed as follows.

An invention is unpatentable if the differences between it and the prior art would have been obvious at the time of the invention. As stated in MPEP § 2143, there are three requirements to establish a *prima facie* case of obviousness.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck* 947 F.2d 488, 20 USPQ2d, 1438 (Fed. Cir. 1991).

Kim describes a MOS transistor that uses a high-k dielectric layer 208. The point of novelty appears to be that Kim uses a silicon oxide gate insulator 202 both above and below the high-k dielectric layer (col. 5, ln. 41-56, Fig. 1). Kim uses a conventional Si channel in Si substrate. The triple insulator layers of SiO2/High-k/SiO2 in the gate stack are for the purpose of reducing leakage current.

Currie describes a transistor where the gate electrode is made from a relaxed SiGe [10-12]. In paragraph [30], Currie mentions that a doped Si channel is formed in the Si well (Fig. 1). Thus, Currie also uses a conventional Si channel in Si substrate. The novelty of the patent appears to be in the use of SiGe.

Sohn, in the description of Figs. 6A through 6E, describes an epi layer of Si 36 that is epitaxially grown over a Si doping layer 35A (col.

7, ln. 46-59). As with Kim and Currie, the channel is Si, formed in a Si well. The novelty is in the use ultra shallow super-steep-retrograde epi-channel by decaborane doping process, as an alternative to an ultra low energy ion implantation technique, to enhance manufacturing productivity.

Unlike the three above-mentioned references, which form transistors on a Si substrate, Hoffman describes a process of fabricating a bottom gate transistor over a glass substrate. Hoffman is included as a reference because he mentions that ZnO may be used as channel material [28, 30, 42, and 48-49]. Hoffman describes a different technical field and different device than any of the other references.

Rotondaro describes a high-k dielectric selective etching process, and is included as a reference because he mentions a high-k dielectric thickness of more than 1 nm.

With respect to the first *prima facie* requirement, there must be some suggestion in the combination of references, that the references can be modified in a manner that would make the claimed invention obvious. The Office Action states that the motivation to combine references is to have a semiconductor device with increased performance. The Applicant respectfully submits that this statement provides absolutely no support for motivation. Alternately stated, if this statement were an actual proof of motivation, then it would support the combination of any group of references, for any purpose.

Kim describes a transistor made with an oxide/high-k dielectric/oxide gate insulator. Currie describes a doped channel layer in the Si well. However, it is not clear that a doped channel can be made to work with an oxide/high-k dielectric/oxide gate insulator. Likewise, it is

not clear how Sohn's epi channel layer can be combined with an oxide/high-k dielectric/oxide gate insulator.

The Kim, Sohn, and Currie references describe building top gate transistors on a Si substrate. Hoffman describes a bottom gate transistor built on a glass substrate. There appears to be no nexus between Hoffman and any of the other references, and the introduction of Hoffman appears to be an attempt to introduce the ZnO material without any consideration of how such a transistor could be integrated with the other references.

From the perspective of the second *prima facie* requirement, even if an expert were given the prior art references as a starting point, there is little expectation of success in the claimed invention. For reasons described below, even if there was a motivation to combine the references, the combination does not yield all the limitations of claims 1 and 13. That is, the combination would not yield all the elements required by the claimed invention.

With respect to the third *prima facie* requirement, the combination of references does not include all the limitations recited in claims 1 and 13. None of the references describe a metal oxide surface channel that is formed over the surface of a Si well. More specifically, none of the references describes the placement of the claimed invention surface channel. As can be seen in Applicant's Fig. 1, Claims 1, 13, and 24 describe a Si well 106 with a surface 108. The claimed invention surface channel 110 overlies the Si well surface 108. Kim, Currie, Sohn, and Rotondaro all describe channels that are formed in a Si well. That is, these references all describe a Si channel. Despite the fact that Sohn and Currie use the phrase "surface channel", their surface channel is formed

in the Si well, as opposed to overlying the well surface, as recited in claims 1 and 13. Hoffman describes a ZnO channel 130 formed between a gate insulator layer 120 and an interlevel dielectric layer 140. Therefore, none of the references, even when combined, describe the limitation of a metal oxide surface channel formed over the surface of a Si well. The combination of references does not explicitly describe all the limitations of claims 1, 13, and 24. Neither does the combination suggest any modifications that would make this limitation obvious. Claims 9, dependent from claim 1, and claim 21, dependent from claim 13, enjoy the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

It is believed that the application is in condition for allowance and reconsideration is earnestly solicited.

Respectfully submitted,

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